

## **REMARKS/ARGUMENTS**

The Applicant would like to acknowledge, with thanks, the Office Action mailed April 19, 2006. This Amendment is responsive to the April 19, 2006 Office Action.

The Examiner acknowledged in the April 19, 2006 Office Action that claim 33 was directed to allowable subject matter. Claim 33 was objected to for depending upon a rejected base claim and would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Accordingly, claim 33 has been canceled and claim 34 is the equivalent of claim 33 rewritten in independent form, including all of the limitations of the base claim and any intervening claims. Therefore, claim 34 should be in condition for allowance. Claims 35-38 depend on claim 34 and therefore contain each and every element of claim 34 and should thus be allowable for the same reasons as claim 34. Claims 39-43 are directed to means for performing the method of claims 34-38 respectively, and claims 44-48 to an apparatus configured for performing the method of claims 34-38 respectively and thus should be allowable for the same reasons.

## **CLAIM OBJECTION**

Claim 10 was objected to because the term 'means for' was duplicated. Accordingly, claim 10 has been amended to overcome this defect.

## **CLAIM REJECTIONS**

Claims 1-4, 7-11, 14-15, 17, 23, 24 and 26-32 stand rejected as being anticipated by U.S. Patent Application Publication No. 2003/0093656 to Masse et al. (*hereinafter* Masse).

Independent claims 1, 2, 3, 8, 9 and 10 recite that the count value in the count register does not change (e.g. increment or decrement) until the execution phase for the instruction. By way of review, the present application described instruction execution in two phases, first an instruction fetch phase where the instruction is fetched, and second an execution phase where the operation specified by the instruction is performed. Masse, which is a pipelining architecture, executes instructions through a 7 stage (phase) pipeline described in Fig. 5 (§ 53). The instruction is fetched at stage P1( § 55), the address of the data to be used in the instruction is

computed during the address phase P3( ¶ 58) and the instruction is executed during stage P6 (¶ 63). Unlike claims 1-3 and 8-10 which recite the counter is updated during the execution phase, the loop counter in Masse “is tested, decremented and updated during the address stage P3 of the pipeline” (¶ 96). “When the single repeat instruction has terminated, i.e. loop counter 922 value=0 at 1110, the rest of the repeat block is executed” (*Id.*). Because of this, Masse has a latency of four instruction cycles (¶ 94). In other words, the counter is being decremented before the single instruction to be executed has started executing. Thus, Masse does not teach that the counter is updated during an execution phase and therefore Masse does not teach every element of claims 1-3 and 8-10.

Claims 4, 7, 31 and 32 depend from claim 3 and therefore contain each and every element of claim 3. Claims 11 and 14 depend from claim 10 and therefore contain each and every element of claim 10. Claims 17, 23 and 24 depend from claim 15 and therefore contain each and every element of claim 15. Claims 26-28 depend from claim 8 and therefore contain each and every element of claim 8. Claims 29 and 30 depend from claim 2 and therefore contain each and every element of claim. Therefore, for the reasons already set forth for claims 1-3 and 8-10, claims 4, 7, 11, 14, 17, 23, 24, 26-28, 29-31 and 32 are not anticipated by Masse.

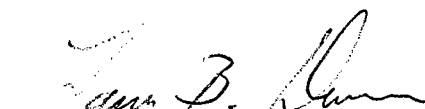
Independent claim 15 recites that the next instruction is not fetched until after the single instruction has repeatedly executed. By contrast, Masse shows that the next instruction (see RPT marked 1112 in Fig. 11) is being fetched while the single instruction (marked as 1108) is at stage P6, the execute step. Therefore, Masse does not teach every element of claim 15.

### **CONCLUSION**

For the reasons just set forth, the claim objection and rejections have been traversed and the claims as they currently stand should be in condition for allowance, and thus a Notice of Allowance is earnestly solicited. If there are any fees necessitated by the foregoing communication, please charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. 72255/02662.

Respectfully submitted,  
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